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Analysis of Transmeta Corporation's Microprocessor Patents

New Issuance Report

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Background

The surging popularity of mobile Internet computing devices, from laptops to PDAs, has created a high demand for microprocessors that use less power, offer high performance, and maintain compatibility with existing x-86 technology. Transmeta Corporation (Nasdaq: TMTA) offers a line of processors to compete in this market segment against such industry heavyweights as Intel and Advanced Micro Devices.

Since its formation in 1995, the Santa Clara, CA-based Transmeta Corporation has been the focus of much debate surrounding the future of microprocessor design. The company was founded by high-profile Silicon Valley personalities David Ditzel (formerly with Bell Labs and Sun) and Paul Allen (co-founder, Microsoft) and counts Linus Torvalds (Linux pioneer) among its principals.

Transmeta's line of Crusoe™ processors, TM3200, TM5400, and TM5600 incorporate the company's patented technologies for microprocessor design. According to the company, the Crusoe™ processors are "a revolutionary x86-compatible family of solutions specially designed for the new world of Mobile Internet Computing."

Transmeta states that the Crusoe™ microprocessor innovation uses software to perform certain processor functions typically reserved for hardware. The Crusoe™ processor is composed of two components, a very-long-instruction-word (VLIW) processor and Code Morphing™ software. These components work together to dynamically translate x86 instruction sets.

[*VLIW is a type of processor architecture; x86 refers to the Intel 8086 family of processors widely used in PCs.*]

The company claims the processors deliver three important features for the mobile computing environment, namely:

- low power consumption,
- low heat generation that eliminates the need for fan cooling, and
- compatibility with the x86-based operating systems.

Beginning with their first patent filings in July of 1996, Transmeta has been working to secure the intellectual property rights that drive their Crusoe™ line of processors, in particular the use of hybrid hardware-software techniques in microprocessor design.

Patent Information

Transmeta holds the following patents for microprocessor design:

Patent Number	Description	Filed	Issued
6172925	Memory array bitline timing circuit	6/14/99	1/9/01
6031992	Combining hardware and software to provide an improved microprocessor	7/5/96	2/29/00
6011908	Gated store buffer for an advanced microprocessor	12/23/96	1/4/00
5958061	Host microprocessor with apparatus for temporarily holding target processor state	7/24/96	9/28/99
5926832	Method and apparatus for aliasing memory data in an advanced microprocessor	9/26/96	7/20/99
5905855	Method and apparatus for correcting errors in computer systems	2/28/97	5/18/99
5832205	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature of a component being addressed	8/20/96	10/3/98
Intel patents developed concurrently with Transmeta Pat. No. 5832205			
5860017	Processor and method for speculatively executing instructions from multiple instruction streams indicated by a branch instruction	6/28/96	1/12/99
5721927	Method for verifying continuity of a binary translated block of instructions by attaching a compare and/or branch instruction to predecessor block of instructions	8/7/96	2/24/98

Financial Information

Transmeta Corporation (Nasdaq: TMTA)

IPO Information	***Key Financials 2000***	***Underwriters***
Filing Date: August 17, 2000	Sales: $ 16.2 million	Morgan Stanley Dean Witter
Date of IPO: November 7, 2000	Net Income: ($97.7 million)	Deutsche Banc Alex. Brown
Shares Offered: 13 million	Market Cap: $ 3.0 billion (Jan. 1, 2001)	Salomon Smith Barney
Offering Amount: $273 million	EPS: ($2.18)	Banc of America Securities, LLC
		SG Cowen

Analysis

The seminal patent in the Transmeta portfolio is U.S. Patent No. 5832205, entitled *Memory controller for a microprocessor for detecting a failure of speculation on the physical nature of a component being addressed,* filed on August 20, 1996 and issued on October 3, 1998. Because this patent lays out much of the basis for the Crusoe™ microprocessor design, namely a hybrid hardware-software technique to convert x86 programs into VLIW instructions, this Patently Obvious™ report will concentrate on this patent's claims and the concurrent art considerations. [*Concurrent art occurs when related patent applications are being examined by the USPTO at the same time*.]

M-CAM, Inc. analysis of the Transmeta portfolio of patents reveals the existence of several closely related concurrent art claims between the Transmeta patent no. 5832205 and Intel patent no. 5721927. The Intel patent '927 entitled, *Method for verifying continuity of a binary translated block of instructions by attaching a compare and/or branch instruction to predecessor block of instructions* was filed 13 days before '205 and was issued 7 months prior to '205. The concurrent art issues found in the '927 patent may limit the exclusivity and reduce the enforceability of some of the claims found in '205.

***Transmeta's patent '205 describes the Crusoe™ Code Morphing Ô software that achieves the x86 conversion*:**

"Rather than providing hardware to enhance the speed of processing as do all the very fast prior art microprocessors, the improved microprocessor allows a large number of acceleration enhancement techniques to be carried out in selectable stages by the code morphing software."

Patent '205 also explains the hardware component, in claim no. 2:

"A system for controlling access to memory as in claim 1 in which the hardware means comprises:

a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and

a storage position in each storage location of the look-aside buffer."

Intel's patent '927 details a method for performing, via software, a conversion of one instruction language to another.

Patent '927 describes this as follows:

"Computer program statements that have been decoded into machine instructions for a source instruction set, such as the Intel® x86, may undergo a binary translation in order to be executed on a target instruction-set computer (RISC) architecture or the very-long-instruction-word (VLIW) architecture."

Analysis (continued)

While the '927 patent does not specifically outline a hybrid hardware-software technique, patent '927 does offer a software or "computer-implemented" method for translating x86 instructions into VLIW instructions, something Intel refers to as Explicitly Parallel Instruction Computing (EPIC).

A critical component of the Transmeta Code Morphing™ software and embodied in the '205 patent is the use of temporary memory or a look-aside buffer to accelerate the translation process. Similarly, patent '927 describes a method to increase the translation speed through the use of a "special section of memory referred to as the Translated Address Table." The claims listed below serve as an illustration of the similarities between the two patents.

Patent '205 describes the memory component in claim 12 as follows:

" A memory control system for a computer comprising:

- main memory,
- memory-mapped input/output (I/O) devices,
- memory control software for causing commands to affect operations at particular addresses,

a translation lookaside buffer including memory locations for storing virtual addresses which have been recently accessed and translations of those virtual addresses to physical addresses within the computer, at least one memory position for each memory location recording an indication whether the address is assumed to be memory or memory-mapped I/O, a comparator for detecting whether an instruction accessing a virtual address stored in the translation lookaside buffer presumes that the physical address is the same as the indication recorded for the physical address."

Patent '927 describes how to take instructions and place them in the translated address memory in claim 6 and 7 as follows:

6. The computer-implemented method of claim 5, wherein the step of appending the load instruction to the second block of instructions further includes appending a fetch instruction to the second block of instructions, the fetch instruction when executed obtains a memory address for the first block of instructions executable on the target instruction set computer architecture, said memory address for the first block of instructions executable on the target instruction set computer architecture is obtained from a translated address table.

7. The computer-implemented method of claim 6, wherein each entry of the translated address table is exclusive of a memory address for blocks of instructions executable on the source instruction set computer architecture.

Another Intel patent that represents concurrent art to '205 is Intel patent no. 5860017 entitled, *Processor and method for speculatively executing instructions from multiple instruction streams indicated by a branch instruction*. This patent offers an alternative approach to handling VLIW processing. Although the '017 patent addresses somewhat different technological issues, such as speculative execution, it represents another example of Intel's concurrent art activity and their effort to build upon the innovations in the area of dynamic translation of execution code.

In addition to Intel, several other competitors have realized the value in applying hardware-software hybrids and the need to improve microprocessor performance. Some competitors/products that will likely continue innovation in this area include: Elbrus/E2K processor, HP/Dynamo Project, and IBM/DAISY processor.

Conclusion

The Crusoe™ processors rely (in part) on their hybrid hardware-software innovation(s) to achieve their low power consumption, small size, and x86 compatibility. While Transmeta holds several patents on these and similar innovations, there is concurrent art, such as the Intel patents analyzed in this report, which may limit the exclusivity of Transmeta's innovation(s).

Transmeta currently enjoys some market advantage in the low-power, x86 compatible, mobile microprocessor market due to the superior operating specifications of their Crusoe™ processors. However, the company faces competition from several large competitors, such as Intel, that have developed and/or are developing technologies to compete with Transmeta's patented innovations.